



# 1 pC Charge Injection, 100 pA Leakage CMOS $\pm 5$ V/+5 V/+3 V Dual SPDT Switch

## ADG636

### FEATURES

- 1 pC Charge Injection
- $\pm 2.7$  V to  $\pm 5.5$  V Dual Supply
- +2.7 V to +5.5 V Single Supply
- Automotive Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- 100 pA (Max @  $25^{\circ}\text{C}$ ) Leakage Currents
- 85  $\Omega$  Typ On Resistance
- Rail-to-Rail Operation
- Fast Switching Times
- Typical Power Consumption ( $<0.1$   $\mu\text{W}$ )
- TTL/CMOS Compatible Inputs
- 14-Lead TSSOP Package

### APPLICATIONS

- Automatic Test Equipment
- Data Acquisition Systems
- Battery-Powered Instruments
- Communication Systems
- Sample-and-Hold Systems
- Remote Powered Equipment
- Audio and Video Signal Routing
- Relay Replacement
- Avionics

### GENERAL DESCRIPTION

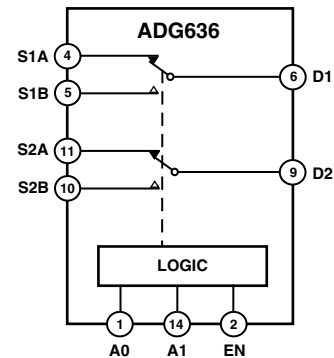
The ADG636 is a monolithic device, comprising two independently selectable CMOS SPDT (Single Pole, Double Throw) switches. When on, each switch conducts equally well in both directions.

The ADG636 operates from a dual  $\pm 2.7$  V to  $\pm 5.5$  V supply, or from a single supply of +2.7 V to +5.5 V.

This switch offers ultralow charge injection of  $\pm 1.5$  pC over the entire signal range and leakage current of 10 pA typical at  $25^{\circ}\text{C}$ . It offers on-resistance of 85  $\Omega$  typ, which is matched to within 2  $\Omega$  between channels. The ADG636 also has low power dissipation yet gives high switching speeds.

The ADG636 exhibits break-before-make switching action and is available in a 14-lead TSSOP package.

### FUNCTIONAL BLOCK DIAGRAM



### PRODUCT HIGHLIGHTS

1. Ultralow Charge Injection ( $Q_{\text{INJ}}$ :  $\pm 1.5$  pC typ over full signal range)
2. Leakage Current  $<0.25$  nA max @  $85^{\circ}\text{C}$
3. Dual  $\pm 2.7$  V to  $\pm 5$  V or Single +2.7 V to +5.5 V Supply
4. Automotive Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
5. Small 14-Lead TSSOP Package

REV. 0

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# ADG636—SPECIFICATIONS

**DUAL SUPPLY**<sup>1</sup> ( $V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = -5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ . All specifications  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  unless noted.)

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{SS}$ to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	85			$\Omega$ typ	$V_{DD} = +4.5\text{ V}$ , $V_{SS} = -4.5\text{ V}$ $V_S = \pm 3\text{ V}$ , $I_S = -1\text{ mA}$ , Test Circuit 1
	115	140	160	$\Omega$ max	
On Resistance Match Between Channels ( $DR_{ON}$ )	2			$\Omega$ typ	$V_S = \pm 3\text{ V}$ , $I_S = -1\text{ mA}$
	4	5.5	6.5	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	25			$\Omega$ typ	$V_S = \pm 3\text{ V}$ , $I_S = -1\text{ mA}$
	40	55	60	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$			nA typ	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$ $V_S = \pm 4.5\text{ V}$ , $V_D = \mp 4.5\text{ V}$ , Test Circuit 2
	$\pm 0.1$	$\pm 0.25$	$\pm 2$	nA max	
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$			nA typ	$V_S = \pm 4.5\text{ V}$ , $V_D = \mp 4.5\text{ V}$ , Test Circuit 2
	$\pm 0.1$	$\pm 0.25$	$\pm 2$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$			nA typ	$V_S = V_D = \pm 4.5\text{ V}$ , Test Circuit 3
	$\pm 0.1$	$\pm 0.25$	$\pm 6$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.4	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	2			pF typ	
<b>DYNAMIC CHARACTERISTICS</b> <sup>2</sup>					
Transition Time	70			ns typ	$V_{S1A} = +3\text{ V}$ , $V_{S1B} = -3\text{ V}$ , $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , Test Circuit 4
	100	120	150	ns max	
$t_{ON}$ Enable	100			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	135	170	190	ns max	$V_S = 3\text{ V}$ , Test Circuit 5
$t_{OFF}$ Enable	55			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	80	90	100	ns max	$V_S = 3\text{ V}$ , Test Circuit 5
Break-Before-Make Time Delay, $t_{BBM}$	20			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 3\text{ V}$ , Test Circuit 5
			10	ns min	
Charge Injection	-1.2			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , Test Circuit 7
Off Isolation	-65			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ , Test Circuit 8
Channel-to-Channel Crosstalk	-65			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ , Test Circuit 10
Bandwidth -3 dB	610			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , Test Circuit 9
$C_S$ (OFF)	5			pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)	8			pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	8			pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
			1.0	$\mu\text{A}$ max	
$I_{SS}$	0.001			$\mu\text{A}$ typ	Digital Inputs = 0 V or 5.5 V
			1.0	$\mu\text{A}$ max	

## NOTES

<sup>1</sup>Y Version Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

**SINGLE SUPPLY<sup>1</sup>** ( $V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ . All specifications  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  unless otherwise noted.)

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	$V_{DD} = 4.5\text{ V}$ , $V_{SS} = 0\text{ V}$
On Resistance ( $R_{ON}$ )	210			$\Omega$ typ	$V_S = 3.5\text{ V}$ , $I_S = -1\text{ mA}$ , Test Circuit 1
	290	350	380	$\Omega$ max	
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	3			$\Omega$ typ	$V_S = 3.5\text{ V}$ , $I_S = -1\text{ mA}$
		12	13	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$			nA typ	$V_{DD} = 5.5\text{ V}$ $V_S = 1\text{ V}/4.5\text{ V}$ , $V_D = 4.5\text{ V}/1\text{ V}$ , Test Circuit 2
	$\pm 0.1$	$\pm 0.25$	$\pm 2$	nA max	
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$			nA typ	$V_S = 1\text{ V}/4.5\text{ V}$ , $V_D = 4.5\text{ V}/1\text{ V}$ Test Circuit 2
	$\pm 0.1$	$\pm 0.25$	$\pm 2$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$			nA typ	$V_S = V_D = 4.5\text{ V}/1\text{ V}$ , Test Circuit 3
	$\pm 0.1$	$\pm 0.25$	$\pm 6$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.4	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	2			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
Transition Time	90			ns typ	$V_{S1A} = 3\text{ V}$ , $V_{S1B} = 0\text{ V}$ , $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , Test Circuit 4
	150	185	210	ns max	
$t_{ON}$ Enable	135			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	180	235	275	ns max	$V_S = 3\text{ V}$ , Test Circuit 5
$t_{OFF}$ Enable	70			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	105	120	135	ns max	$V_S = 3\text{ V}$ , Test Circuit 5
Break-Before-Make Time Delay, $t_{BBM}$	30			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 3\text{ V}$ , Test Circuit 5
			10	ns min	$V_S = 3\text{ V}$ , Test Circuit 5
Charge Injection	0.3			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , Test Circuit 7
Off Isolation	-60			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ , Test Circuit 8
Channel-to-Channel Crosstalk	-65			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ , Test Circuit 10
Bandwidth -3 dB	530			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , Test Circuit 9
$C_S$ (OFF)	5			pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)	8			pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	8			pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
			1.0	$\mu\text{A}$ max	

## NOTES

<sup>1</sup>Y Version Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ <sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# ADG636

## SINGLE SUPPLY<sup>1</sup> ( $V_{DD} = 3\text{ V} \pm 10\%$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ . All specifications $-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ unless otherwise noted.)

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	380	420	460	$\Omega$ typ	$V_{DD} = 2.7\text{ V}$ , $V_{SS} = 0\text{ V}$ $V_S = 1.5\text{ V}$ , $I_S = -1\text{ mA}$ , Test Circuit 1
On Resistance Match Between Channels ( $\Delta R_{ON}$ )			5	$\Omega$ typ	$V_S = 1.5\text{ V}$ , $I_S = -1\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$			nA typ	$V_{DD} = 3.3\text{ V}$ $V_S = 1\text{ V}/3\text{ V}$ , $V_D = 3\text{ V}/1\text{ V}$ , Test Circuit 2
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.1$	$\pm 0.25$	$\pm 2$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.1$	$\pm 0.25$	$\pm 2$	nA typ	$V_S = 1\text{ V}/3\text{ V}$ , $V_D = 3\text{ V}/1\text{ V}$ , Test Circuit 2
	$\pm 0.1$	$\pm 0.25$	$\pm 6$	nA max	$V_S = V_D = 1\text{ V}/3\text{ V}$ , Test Circuit 3
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
$C_{IN}$ , Digital Input Capacitance	2			$\mu\text{A}$ max pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
Transition Time	170			ns typ	$V_{S1A} = 2\text{ V}$ , $V_{S1B} = 0\text{ V}$ , $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , Test Circuit 4
$t_{ON}$ Enable	320	390	450	ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	250			ns typ	$V_S = 2\text{ V}$ , Test Circuit 6
$t_{OFF}$ Enable	360	460	530	ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	110			ns typ	$V_S = 2\text{ V}$ , Test Circuit 6
Break-Before-Make Time Delay, $t_{BBM}$	175	205	230	ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_{S1} = 2\text{ V}$ , Test Circuit 5
	80			ns typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , Test Circuit 7
Charge Injection	0.6		10	ns min	
Off Isolation	-60			pC typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ , Test Circuit 8
Channel-to-Channel Crosstalk	-65			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ , Test Circuit 10
Bandwidth -3 dB	530			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , Test Circuit 9
$C_S$ (OFF)	5			pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)	8			pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	8			pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001	1.0	$\mu\text{A}$ max	$\mu\text{A}$ typ	$V_{DD} = 3.3\text{ V}$ Digital Inputs = 0 V or 3.3 V

### NOTES

<sup>1</sup>Y Version Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = 25°C unless otherwise noted)

V <sub>DD</sub> to V <sub>SS</sub> .....	13 V
V <sub>DD</sub> to GND .....	-0.3 V to +6.5 V
V <sub>SS</sub> to GND .....	+0.3 V to -6.5 V
Analog Inputs <sup>2</sup> .....	V <sub>SS</sub> - 0.3 V to V <sub>DD</sub> + 0.3 V
Digital Inputs <sup>2</sup> .....	-0.3 V to V <sub>DD</sub> + 0.3 V or 30 mA, Whichever Occurs First

Peak Current, S or D

(Pulsed at 1 ms, 10% Duty Cycle max) ..... 20 mA

Continuous Current, S or D ..... 10 mA

Operating Temperature Range

Automotive (Y Version) ..... -40°C to +125°C

Storage Temperature Range ..... -65°C to +150°C

Junction Temperature ..... 150°C

TSSOP Package

θ<sub>JA</sub> Thermal Impedance ..... 150°C/W

θ<sub>JC</sub> Thermal Impedance ..... 27°C/W

Lead Temperature, Soldering (10 seconds) ..... 300°C

IR Reflow, Peak Temperature ..... 220°C

## NOTES

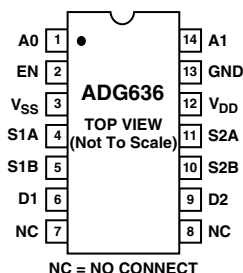
<sup>1</sup> Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

<sup>2</sup> Overvoltages at EN, A0, A1, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG636YRU	-40°C to +125°C	Thin Shrink Small Outline (TSSOP)	RU-14

## PIN CONFIGURATION



**Table I. Truth Table**

A1	A0	EN	ON Switch
X	X	0	NONE
0	0	1	S1A, S2A
0	1	1	S1B, S2A
1	0	1	S1A, S2B
1	1	1	S1B, S2B

## CAUTION

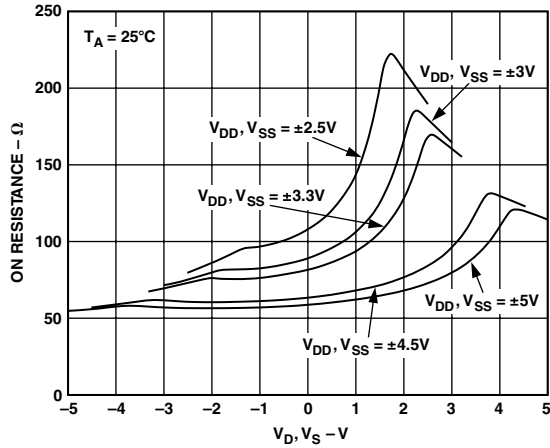
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG636 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



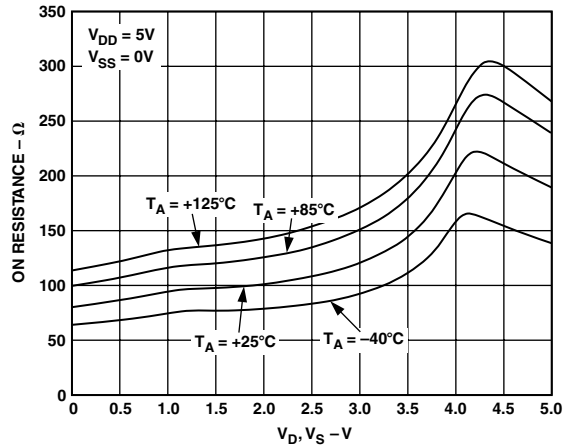
## TERMINOLOGY

$V_{DD}$	Most Positive Power Supply Potential
$V_{SS}$	Most Negative Power Supply in a Dual Supply Application. In single supply applications, this should be tied to ground at the device.
GND	Ground (0 V) Reference
$I_{DD}$	Positive Supply Current
$I_{SS}$	Negative Supply Current
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
$R_{ON}$	Ohmic Resistance between D and S
$\Delta R_{ON}$	On Resistance Match between any two channels (i.e., $R_{ON\ max} - R_{ON\ min}$ )
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of On Resistance as measured over the specified analog signal range.
$I_S$ (OFF)	Source Leakage Current with the Switch “OFF”
$I_D$ (OFF)	Drain Leakage Current with the Switch “OFF”
$I_D, I_S$ (ON)	Channel Leakage Current with the Switch “ON”
$V_D, V_S$	Analog Voltage on Terminals D, S
$V_{INL}$	Maximum Input Voltage for Logic “0”
$V_{INH}$	Minimum Input Voltage for Logic “1”
$I_{INL}(I_{INH})$	Input Current of the Digital Input
$C_S$ (OFF)	Channel Input Capacitance for “OFF” condition.
$C_D$ (OFF)	Channel Output Capacitance for “OFF” condition.
$C_D, C_S$ (ON)	“ON” Switch Capacitance
$C_{IN}$	Digital Input Capacitance
$t_{ON(EN)}$	Delay time between the 50% and 90% points of the digital input and Switch “ON” condition
$t_{OFF(EN)}$	Delay time between the 50% and 90% points of the digital input and Switch “OFF” condition
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital input and Switch “ON” condition when switching from one address state to another.
$t_{BBM}$	“OFF” time or “ON” time measured between the 80% points of both switches, when switching from one address state to another.
Charge Injection	A measure of the Glitch Impulse transferred from the Digital Input to the Analog Output during switching.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an “OFF” switch.
Bandwidth	The Frequency Response of the “ON” Switch
Insertion Loss	Loss Due to the On Resistance of the Switch

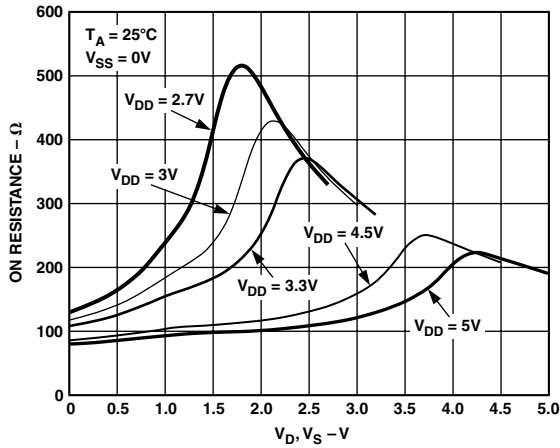
# Typical Performance Characteristics—ADG636



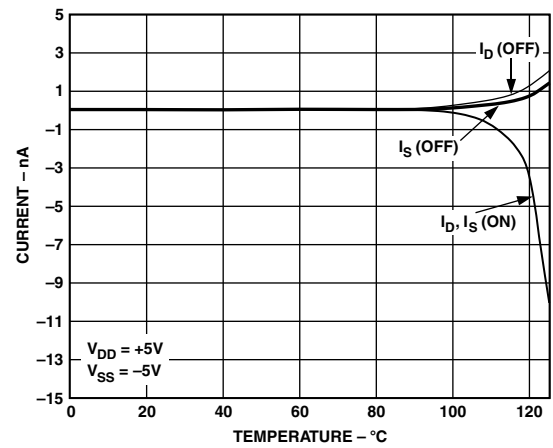
TPC 1. On Resistance vs.  $V_D$  ( $V_S$ ). Dual Supply



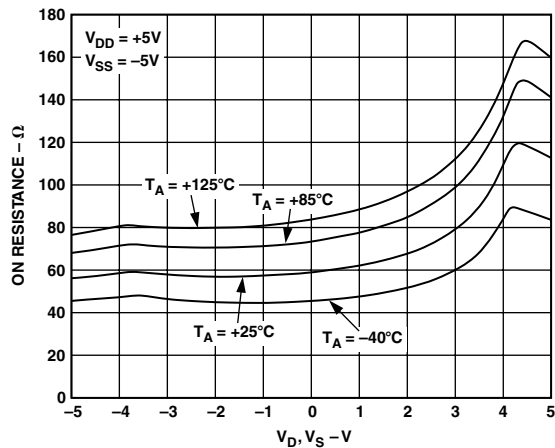
TPC 4. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures. Single Supply



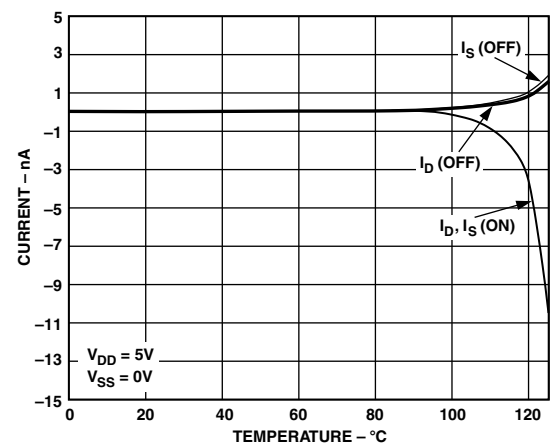
TPC 2. On Resistance vs.  $V_D$  ( $V_S$ ). Single Supply



TPC 5. Leakage Currents vs. Temperatures. Dual Supply

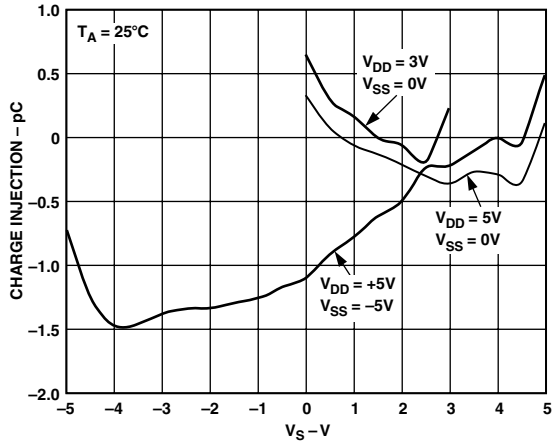


TPC 3. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures. Dual Supply

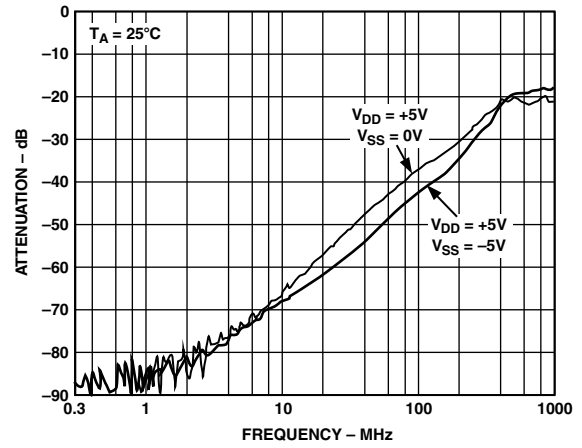


TPC 6. Leakage Currents vs. Temperature. Single Supply

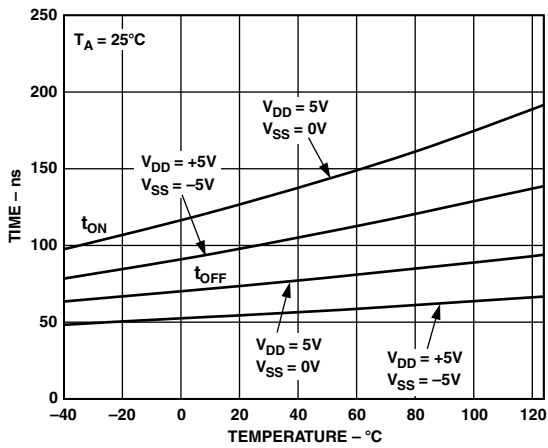
# ADG636



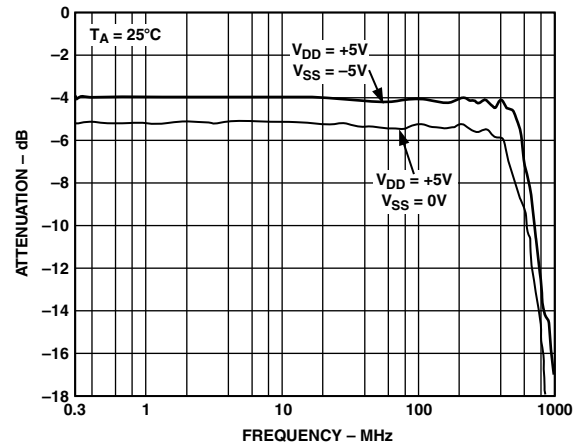
TPC 7. Charge Injection vs. Source Voltage



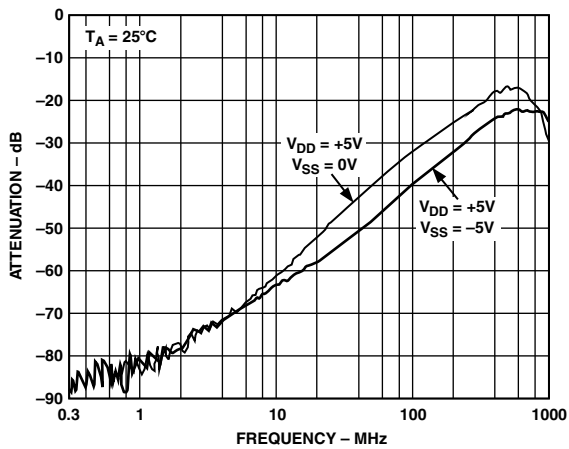
TPC 10. Crosstalk vs. Frequency



TPC 8.  $t_{ON}/t_{OFF}$  Enable Timing vs. Temperature



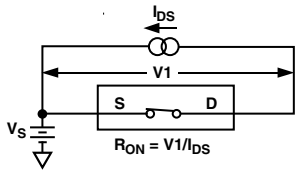
TPC 11. On Response vs. Frequency



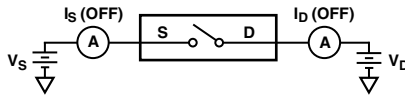
TPC 9. Off Isolation vs. Frequency



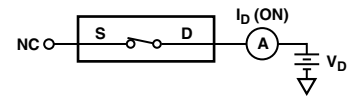
# Test Circuits



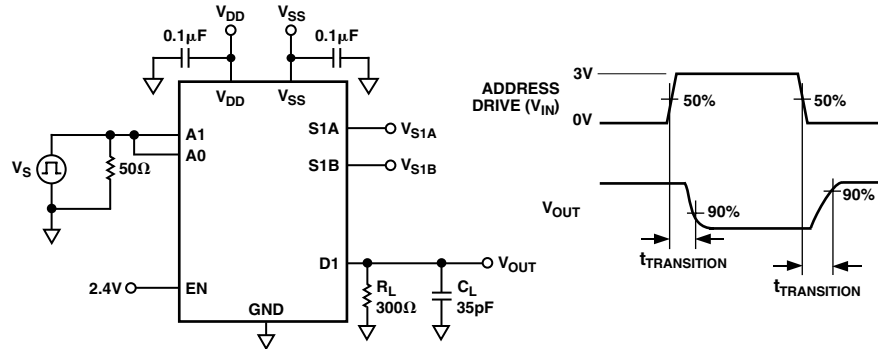
Test Circuit 1. On Resistance



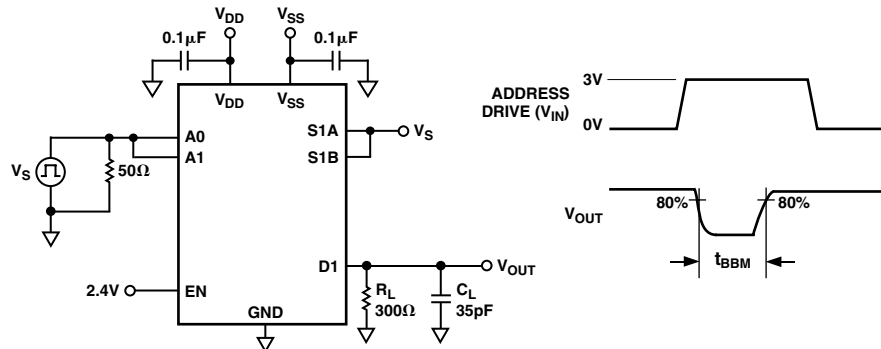
Test Circuit 2. Off Leakage



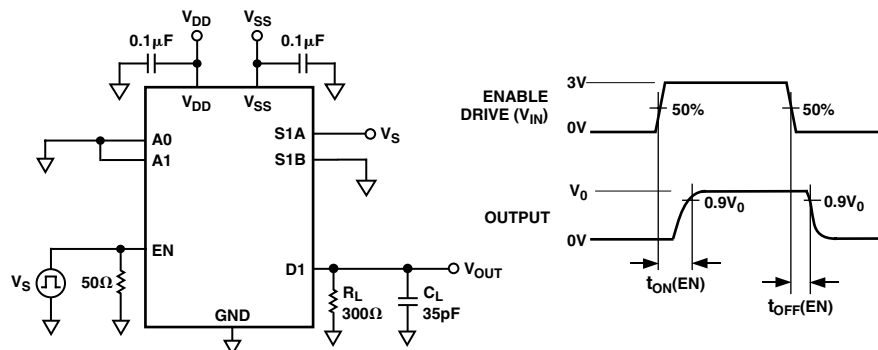
Test Circuit 3. On Leakage



Test Circuit 4. Transition Time,  $t_{TRANSITION}$

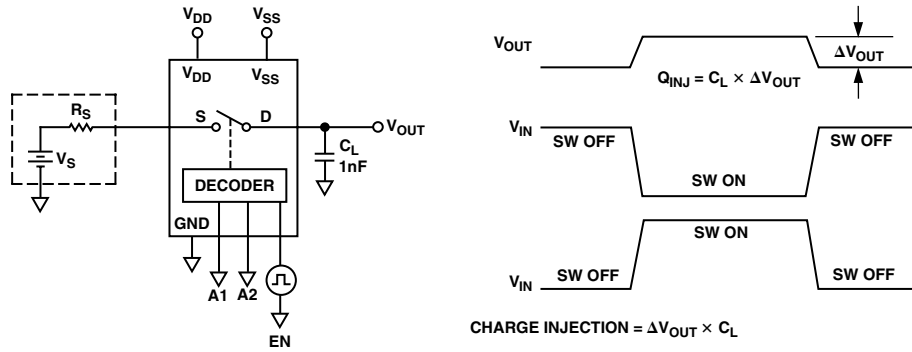


Test Circuit 5. Break-Before-Make Delay,  $t_{BBM}$

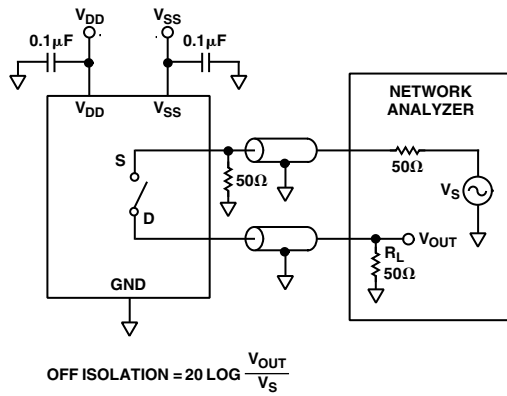


Test Circuit 6. Enable Delay,  $t_{ON}(EN)$ ,  $t_{OFF}(EN)$

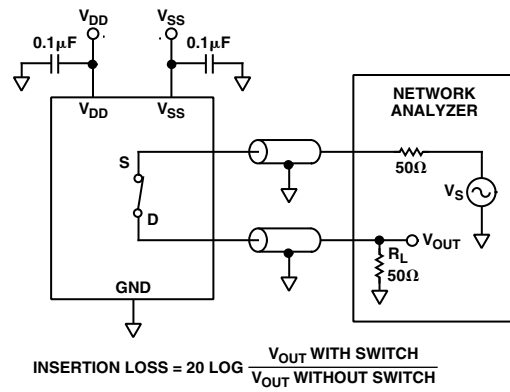
# ADG636



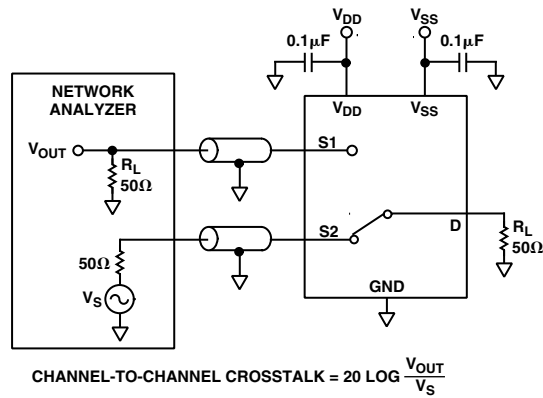
Test Circuit 7. Charge Injection



Test Circuit 8. Off Isolation



Test Circuit 9. Bandwidth



Test Circuit 10. Channel-to-Channel Crosstalk

**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

**14-Lead TSSOP Package  
(RU-14)**

